ABSTRACT OF THE DISCLOSURE

A method for forming a lightly doped drain (LDD) field effect transistor uses very thin first sidewall spacers over the gate sidewalls, in which annealing/oxidation of the sidewall spacers results in (a) the rounding of corner portions of the gate structure sidewalls adjacent the gate oxide, and (b) a very low thermal consumption comprising a small portion of the total thermal budget. Secondary sidewall spacers of greater width are then formed to act as offsets in the introduction of N-type dopants into the substrate to form source and drain contact regions. The method may be varied to accommodate various design configurations and size scaling.